# Scaling Challenges of FinFET Technology at Advanced Nodes & Its impact on SoC design


***Srinivasa R Banna PhD***

***Fellow & Director of Advanced Device Architecture***

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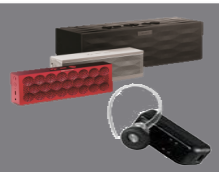
# Outline

- Motivation
- SoC guidelines
- FinFET Scaling
  - Fin Scaling
  - Gate Pitch Scaling
- Future Directions
- Summary

# Motivation (1/3)

## *Market needs drive technology offerings*

- **Wireless**
- **Mobile Computing**
- **Consumer**
- **IoT**



Wireless Connectivity

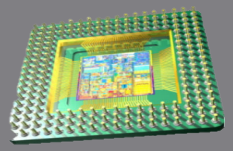
Smartphones

Tablets

Portable consumer


DTV

- **High Performance Computing**



Microprocessors

Game consoles

Networking

- **Wired Applications**
- **Networking**

STB

Graphics

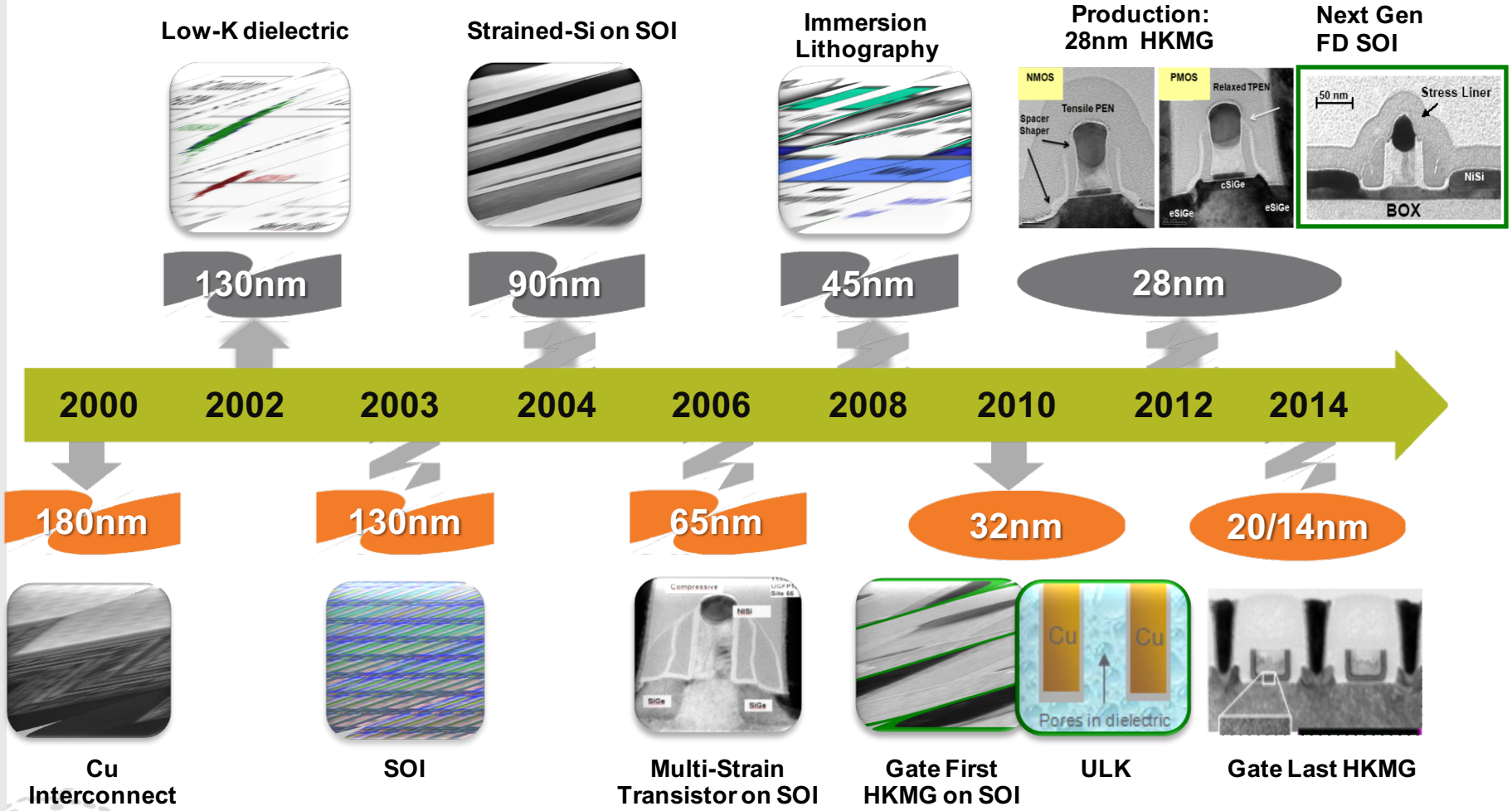

DTV

Networking

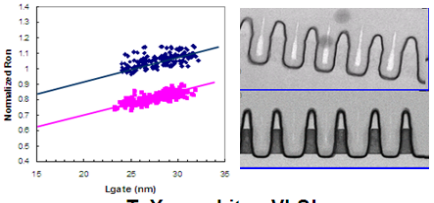
Servers / Storage

# Motivation (2/3)

## *Technology offering drives innovation*



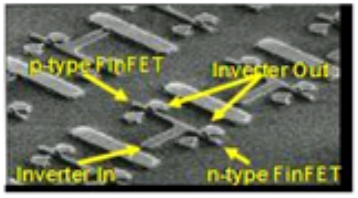
# Motivation (3/3)
## A Decade of FINFET R&D




T. Yamashita , VLSI

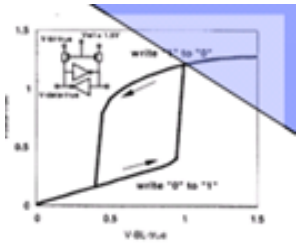


Conformal doping in FinFET (2011)



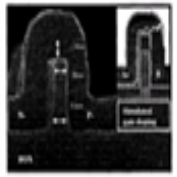

E.Nowak CICC

FinFET fully-depleted RO demo (2003)



E.Nowak IEDM

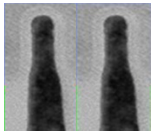
FinFET CMOS demo (2002)

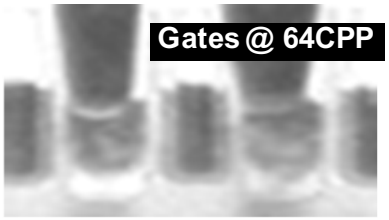


J. Kedzierski IEDM

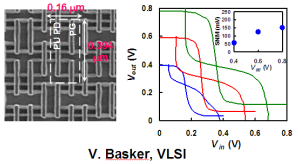
High speed FinFET device N&P (2001)

10nm Platform (2014)



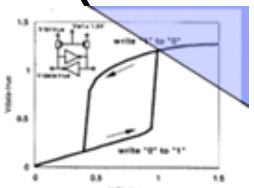



0.063µm² SRAM with FinFET (2010)

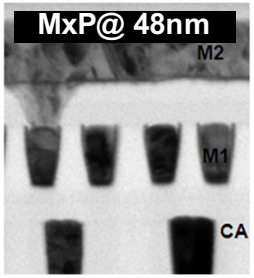


V. Basker, VLSI

Functional SRAM 0.22µm² (2002)

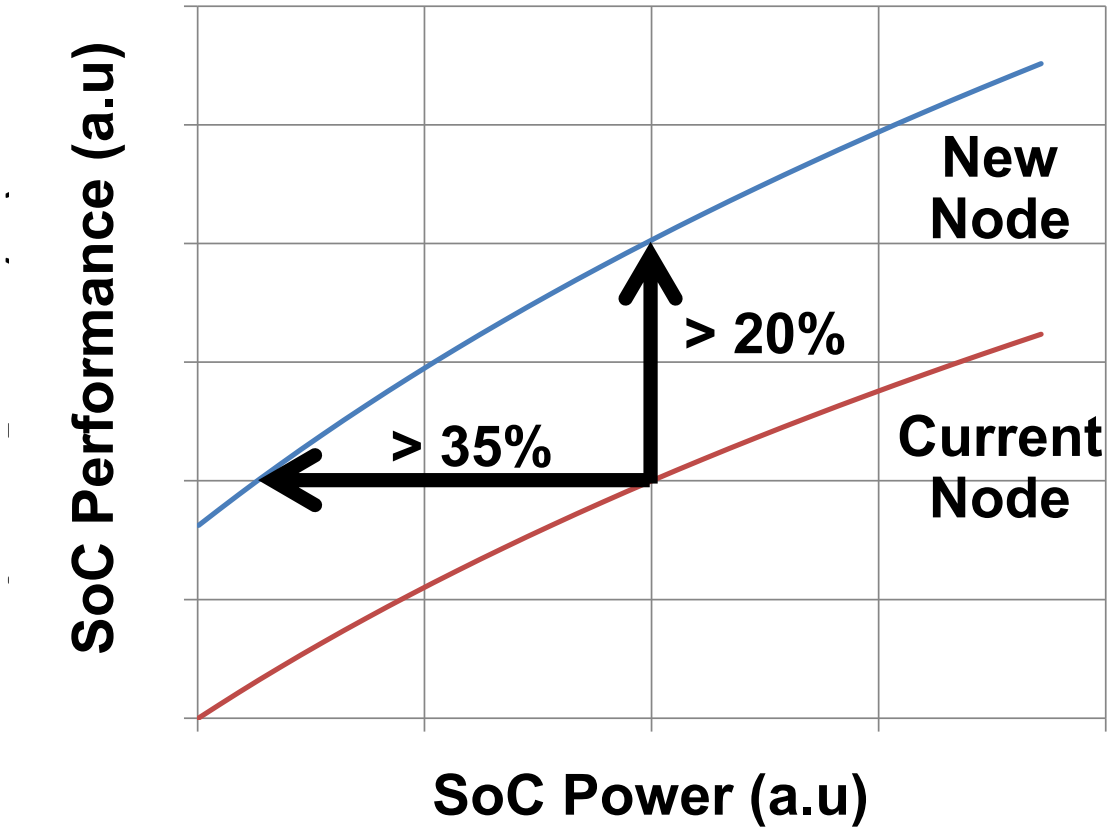


E.Nowak IEDM




K.Seo VLSI

# SoC Guidelines




- ≥ 20% performance uplift at iso power
- ≥ 35% power reduction at iso performance
- Enable lowest Vmin & highest Vmax

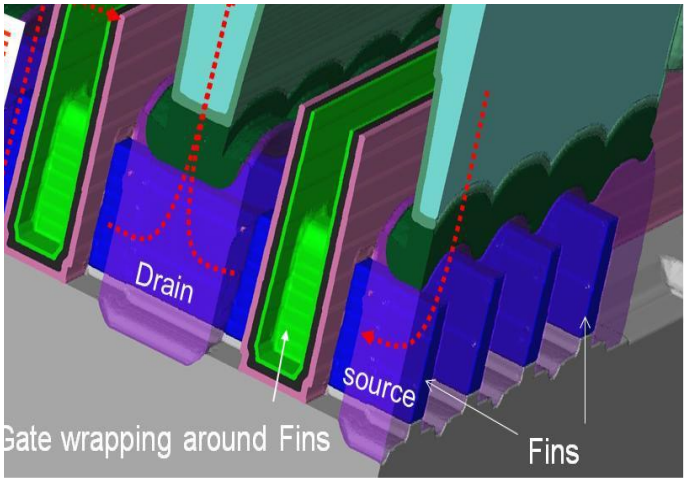
# FinFET Fin Scaling

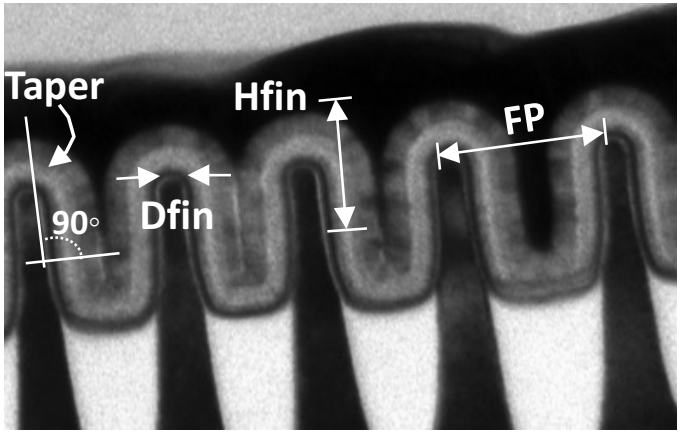
## *Key fin parameters*

- Fin Width (Dfin)
- Fin Taper (Tfin)
- Fin Space (Sfin)
- Fin Height (Hfin)
- Fin Pitch (FP)

Goal : Tighter, thinner and taller fins

**3D FinFET View**

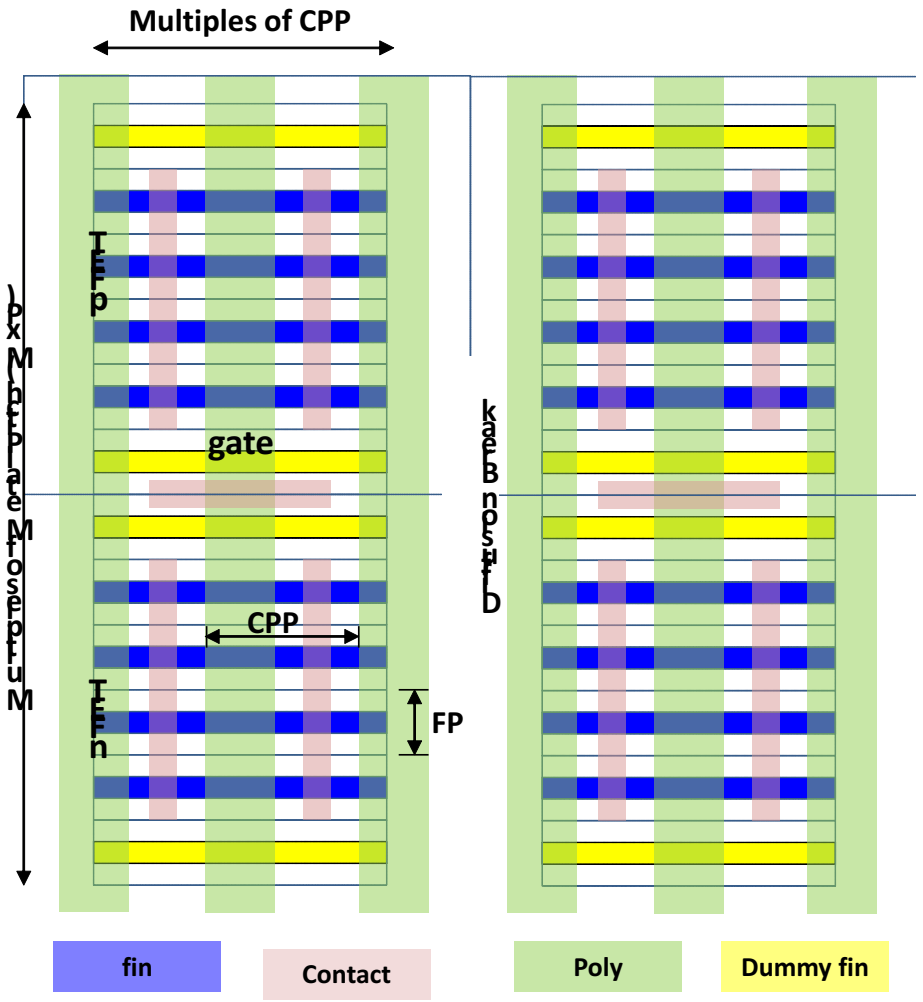



**Along gate direction**

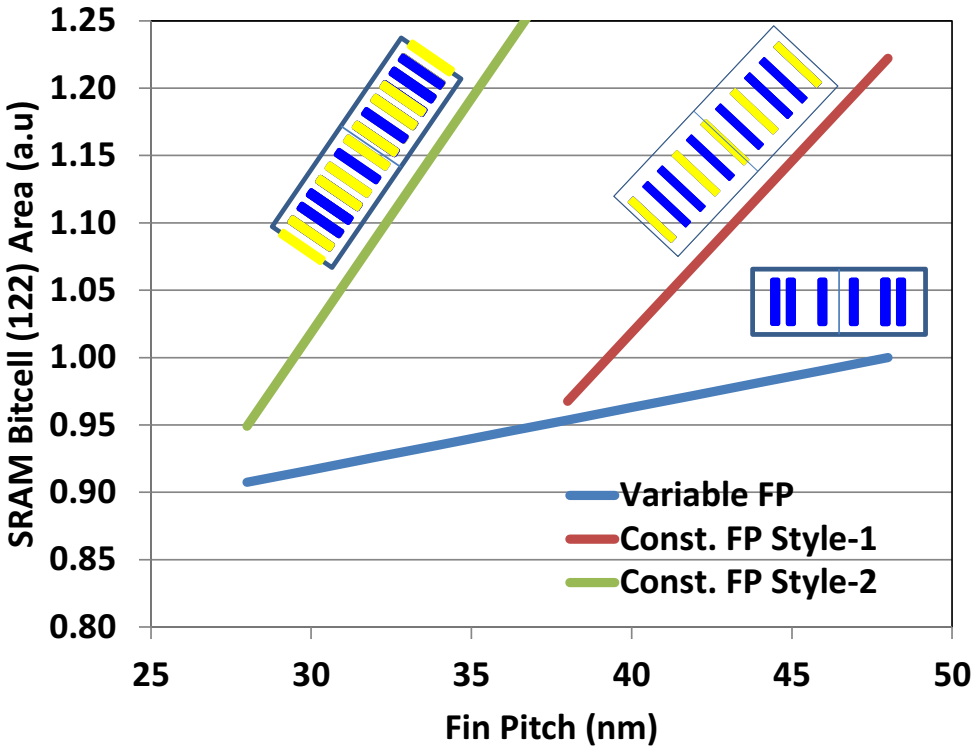
# Fin Pitch Scaling
## *Impact on Std. Cells*

- No. of fins / device
- Middle of Line (MoL) design
- Power Rail (PR) design
- Cell height
- SoC Performance, Power and Area (PPA)



# Fin Pitch Scaling
## *Impact on SRAM*

- # of fins/device
- MoL design
- Bitcell width
- Metal choices for BL, WL, Power supplies

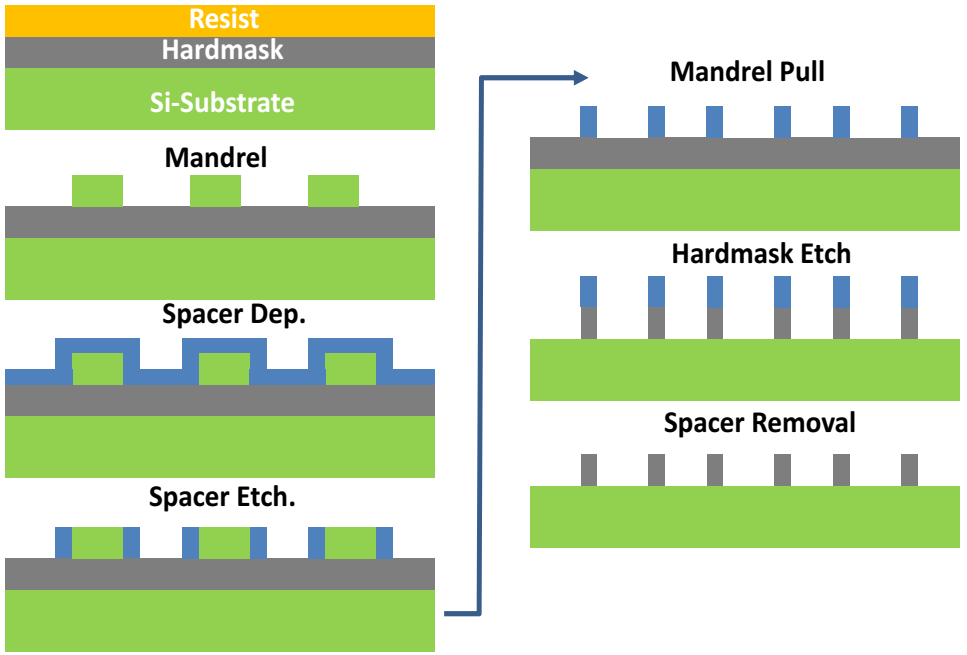



Variable *vs.* Constant FP : Variable FP offers best area scaling

# Fin Pitch Scaling
## *Impact on Lithography*

- Litho cost drives process cost
- Litho choices: SADP[1] or SAQP[2]
- Photoresist, hard mask and spacer material choices

**Typical SADP flow**

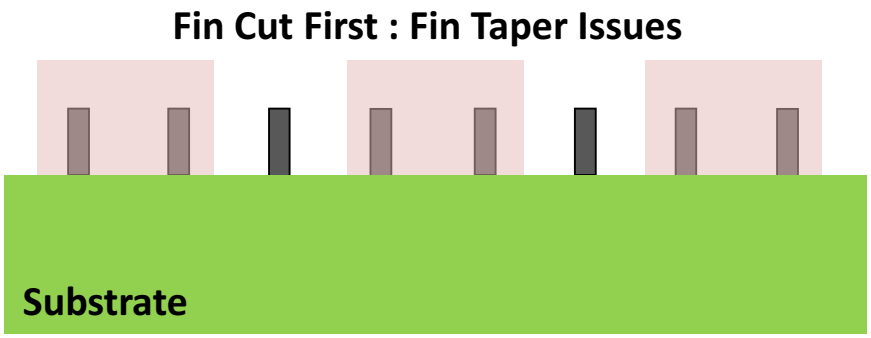


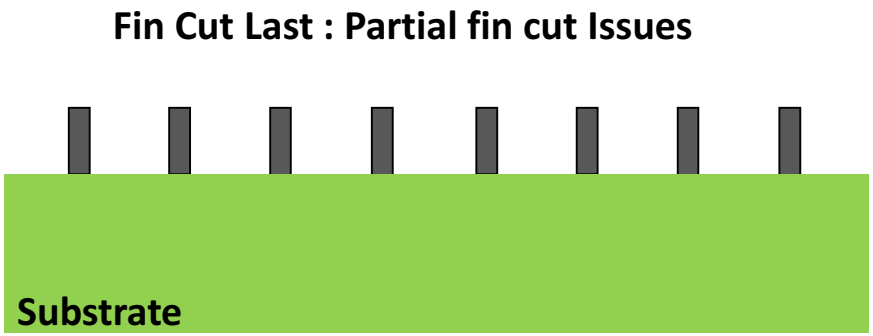

- Fin pitch scaling impact lithography choices and overall process cost

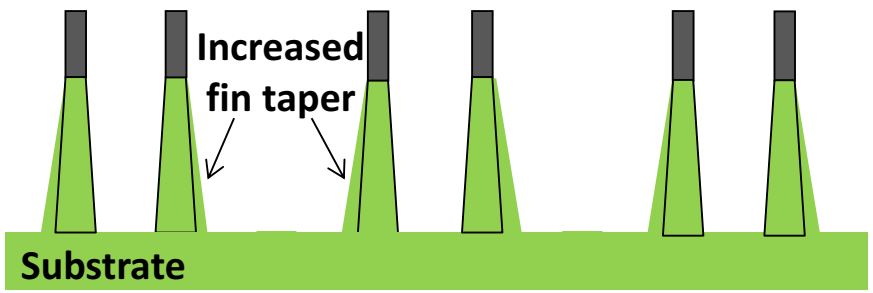
1: Self Aligned Double Patterning
2: Self Aligned Quadruple Patterning

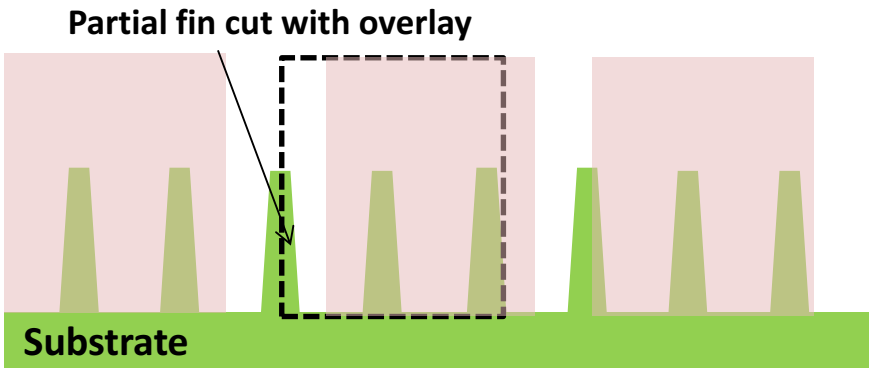
# Fin Pitch Scaling
## *Impact on Fin Variability*

- Fin Cut : *First* or *Last*
- *Fin taper variability* or *partial fin cut*



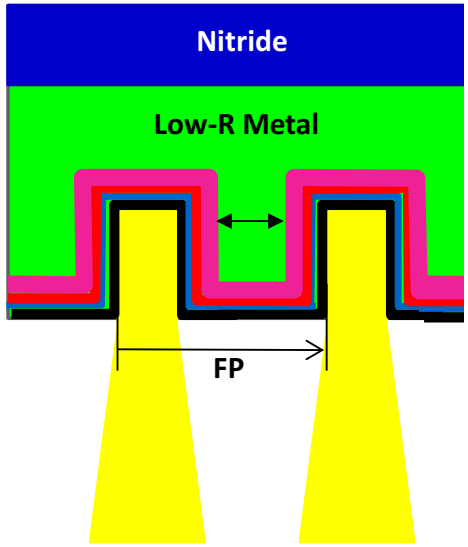



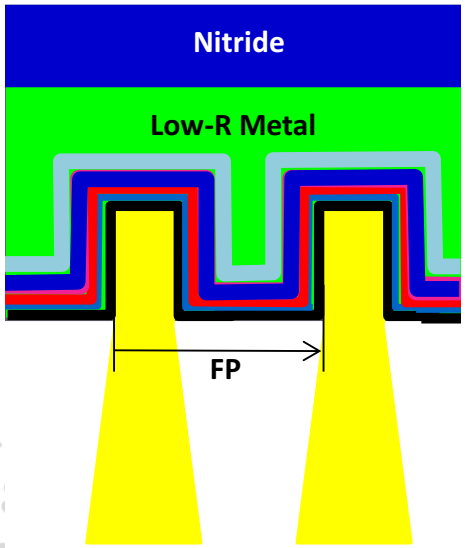



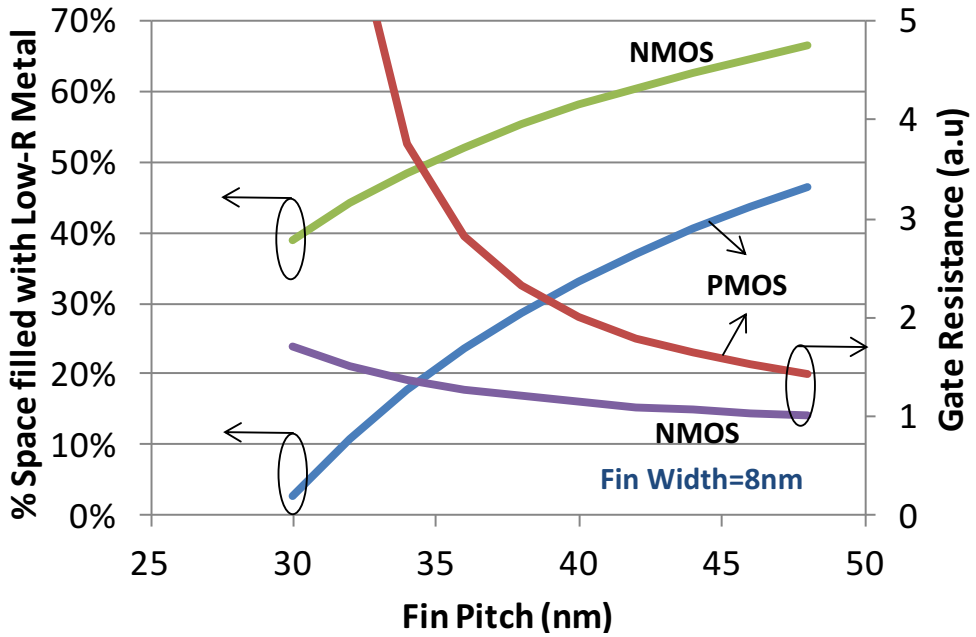



# Fin Pitch Scaling

## *Impact on RMG & IO Device*

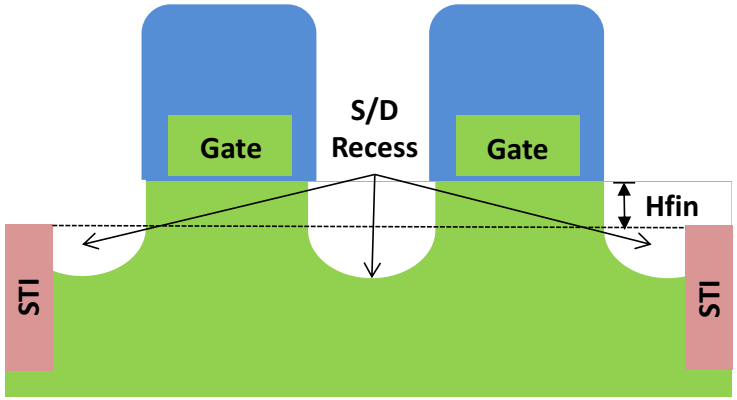


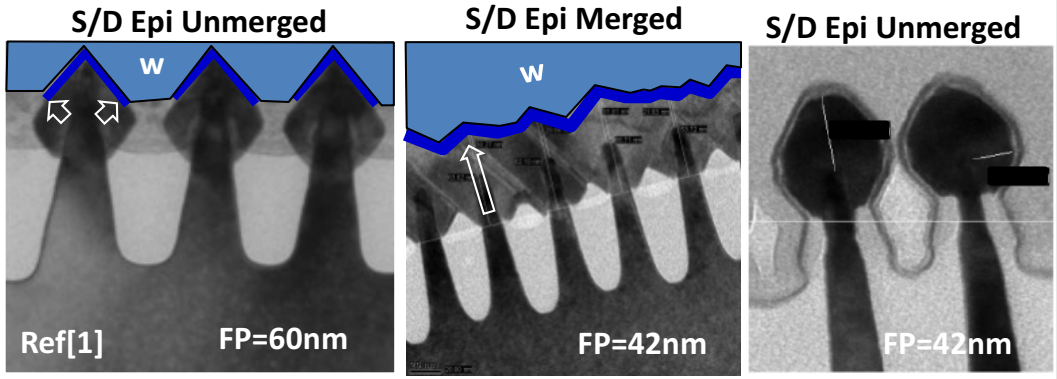



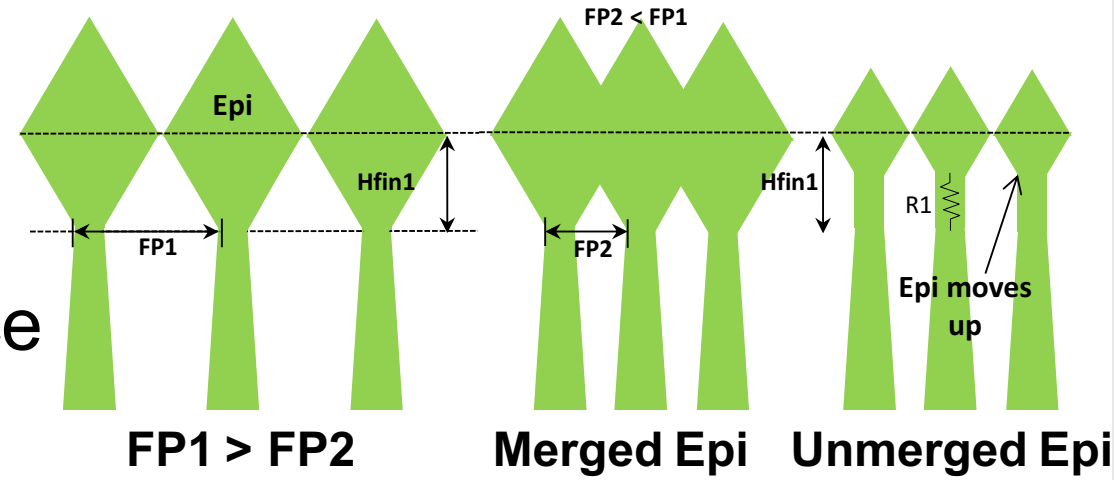

- Gate work function control
- Impacts IO device performance & reliability
- Increased gate resistance hurts analog / RF design

# Fin Pitch Scaling
## *Impact on S/D formation*



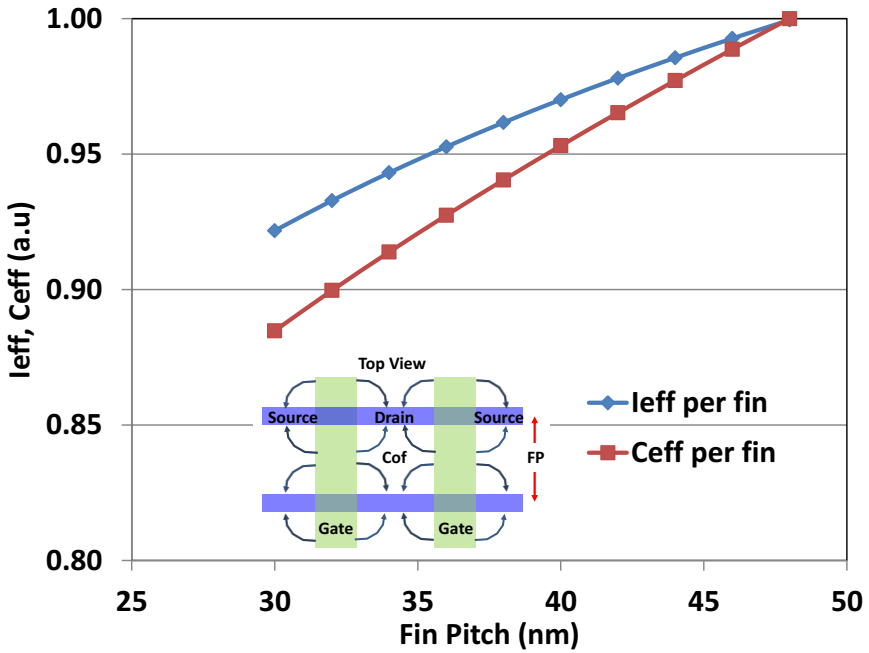



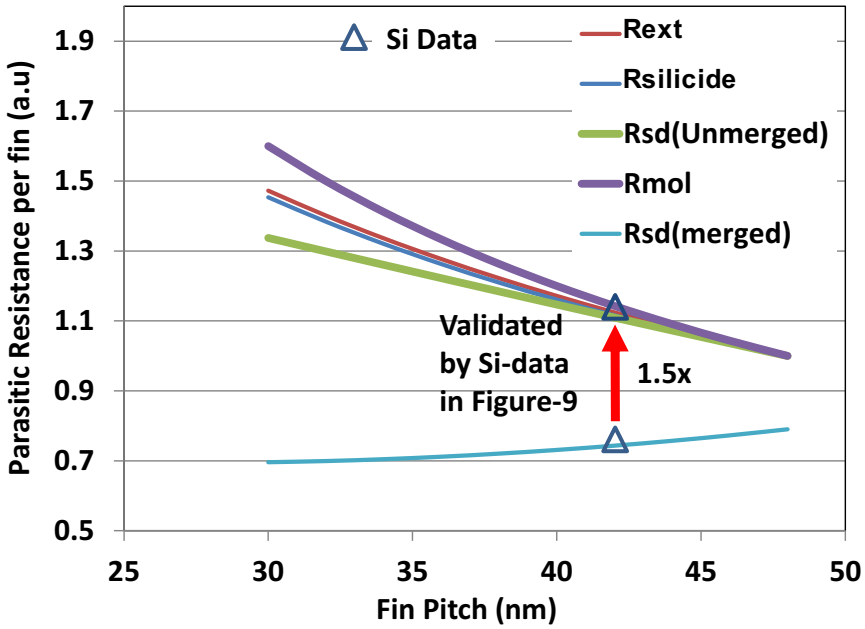

- S/D design is critical for best SoC PPA
- Epi growth is vital
  - Low SD Resistance
  - High chip yield



# Fin Pitch Scaling

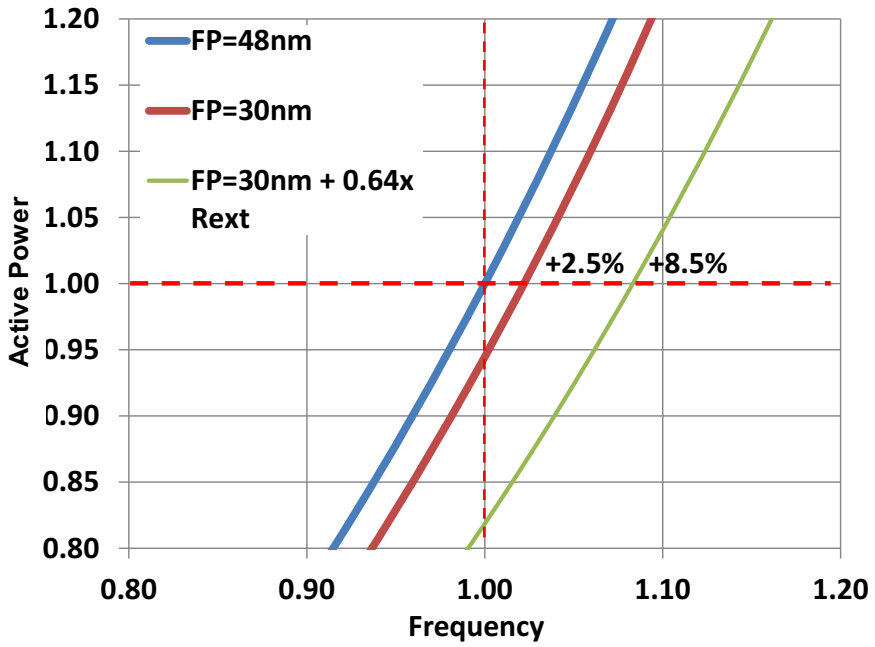
## *Impact on Device*

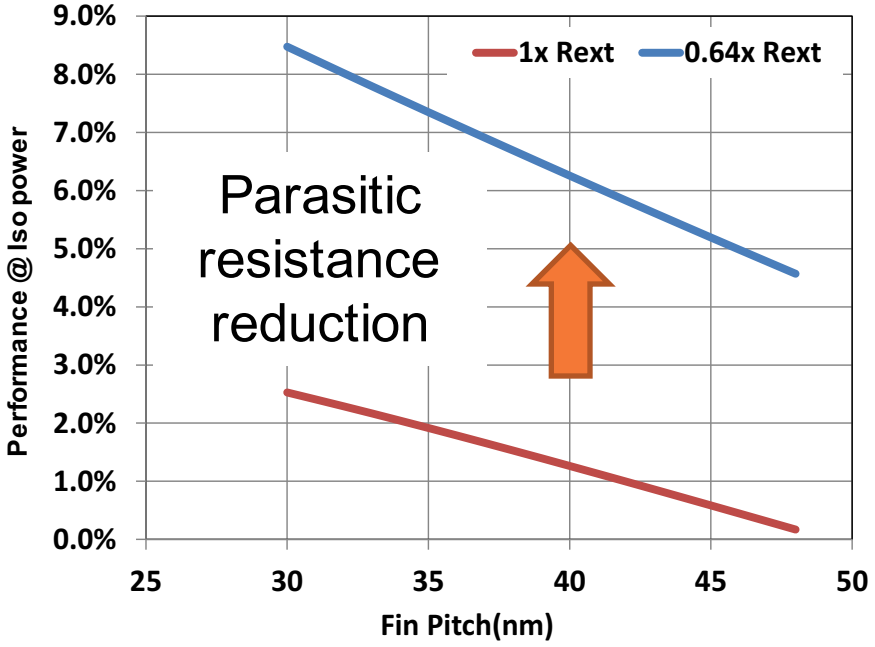



- Ceff reduces due to lower fringing capacitance between the fins
- Ieff reduces due to increase in Rext (Rmol + Rsilicide + Rsd)

# Fin Pitch Scaling
## *Impact on SoC*

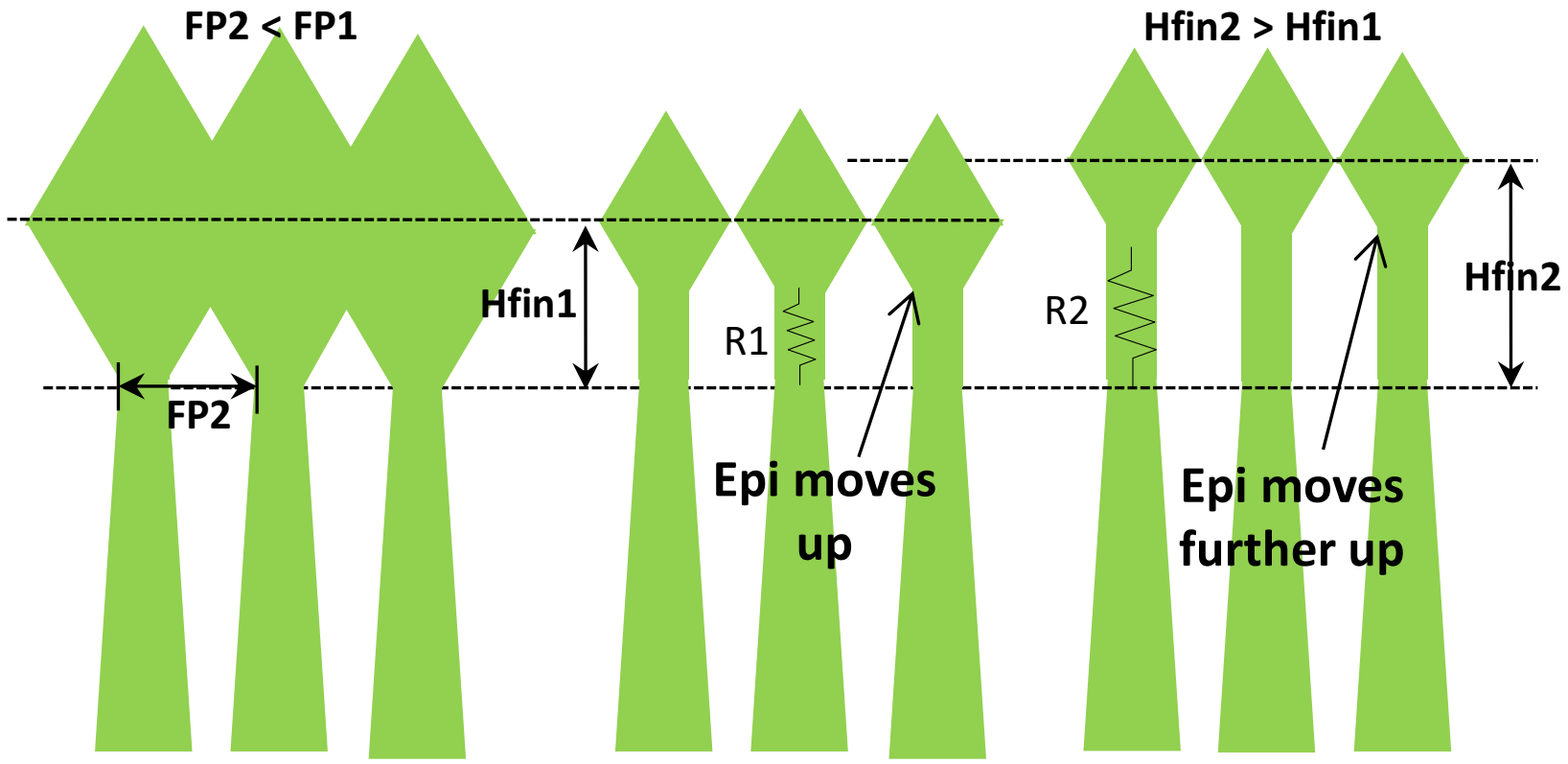



- Significant S/D engineering is required to improve SoC performance @ iso power

# Fin Height Scaling

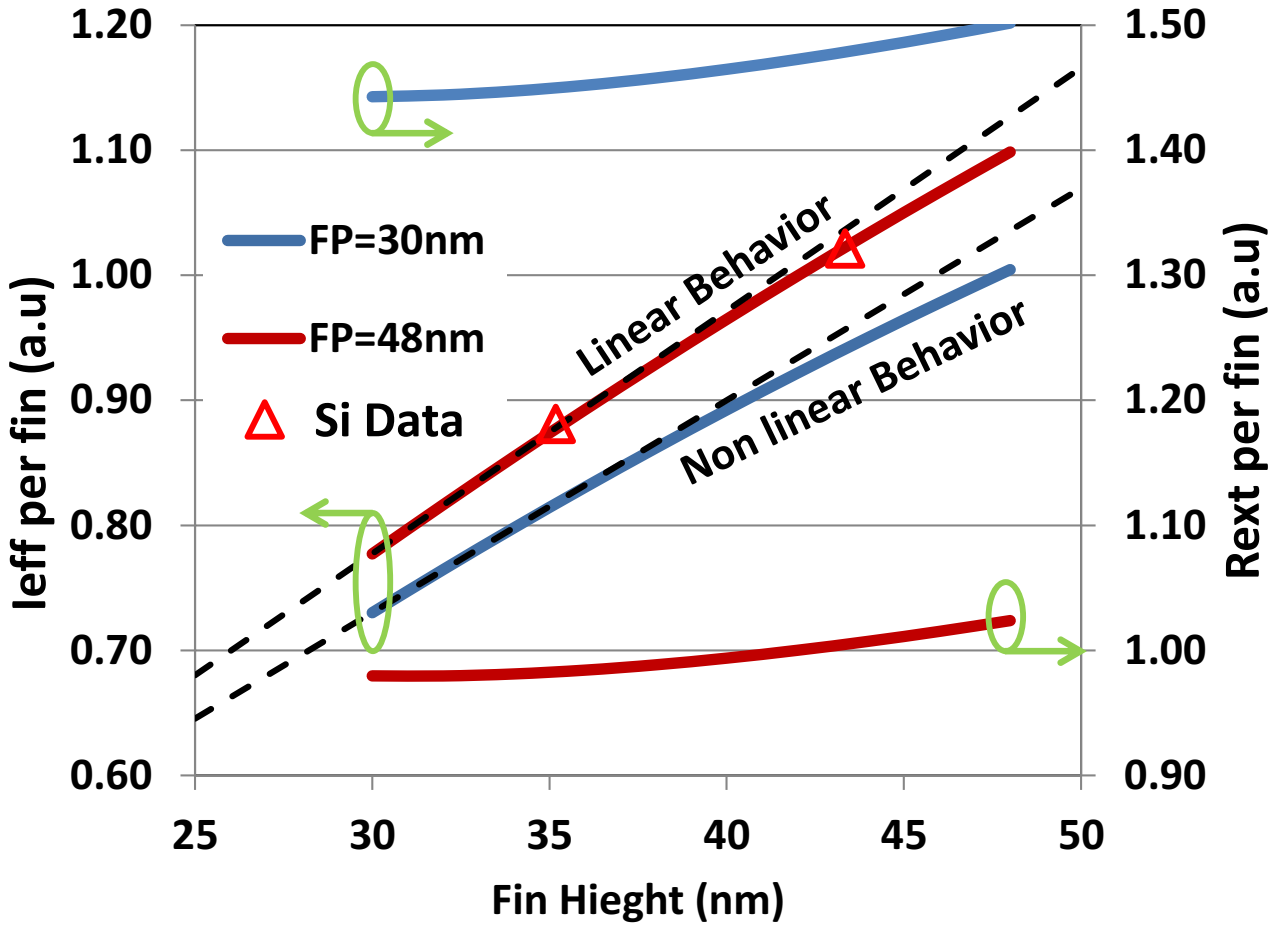
## *Impact on SD formation*




- SD resistance increases with taller fins

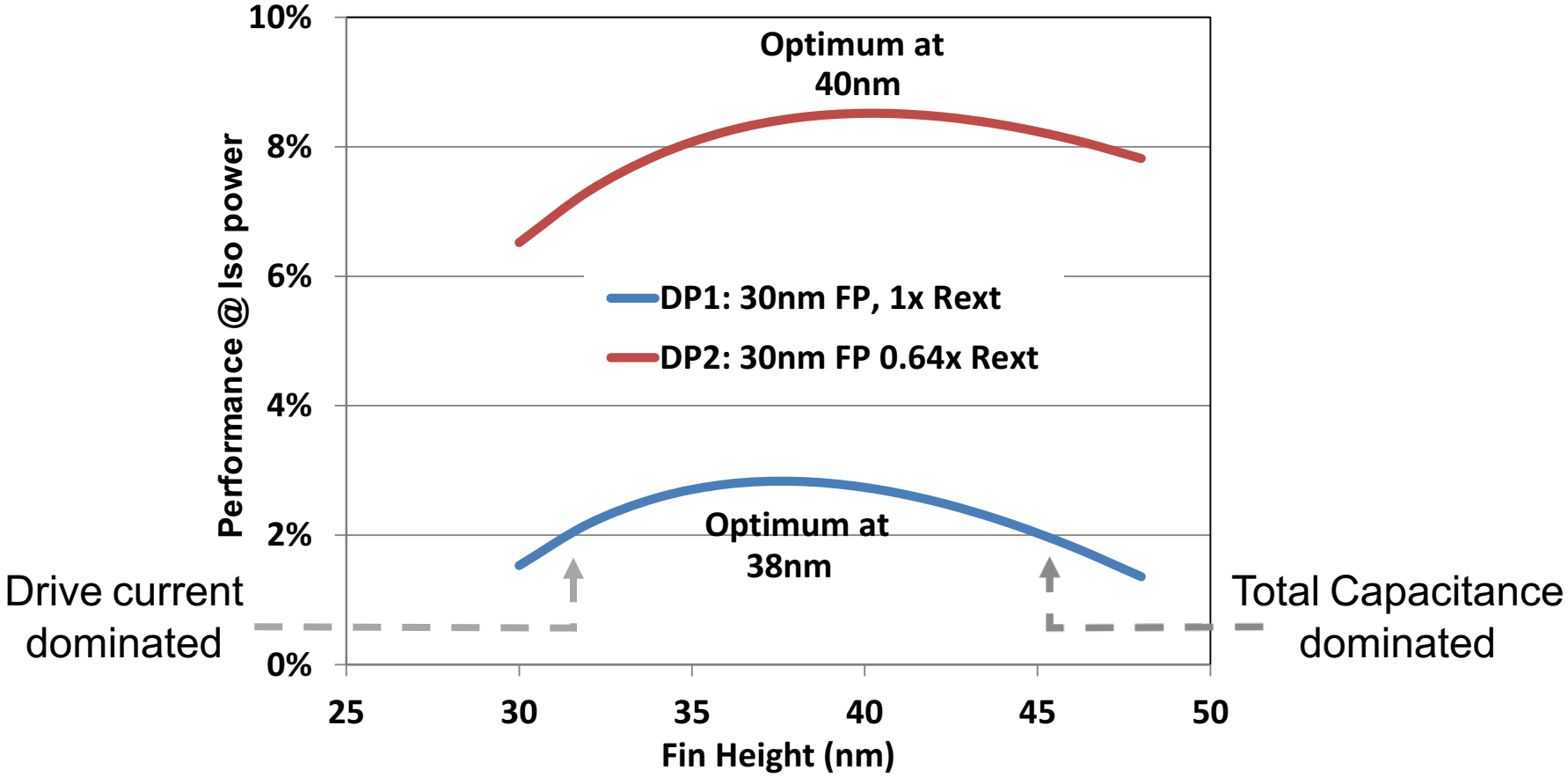
# Fin Height Scaling

## *Impact on Device*



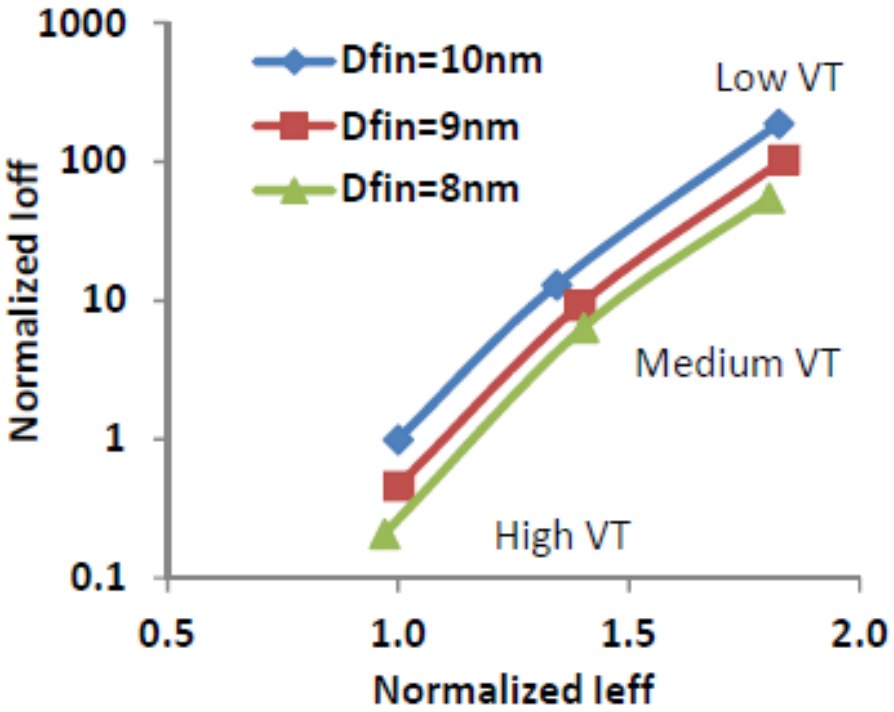

- Diminishing Ieff uplift as fin height is increased

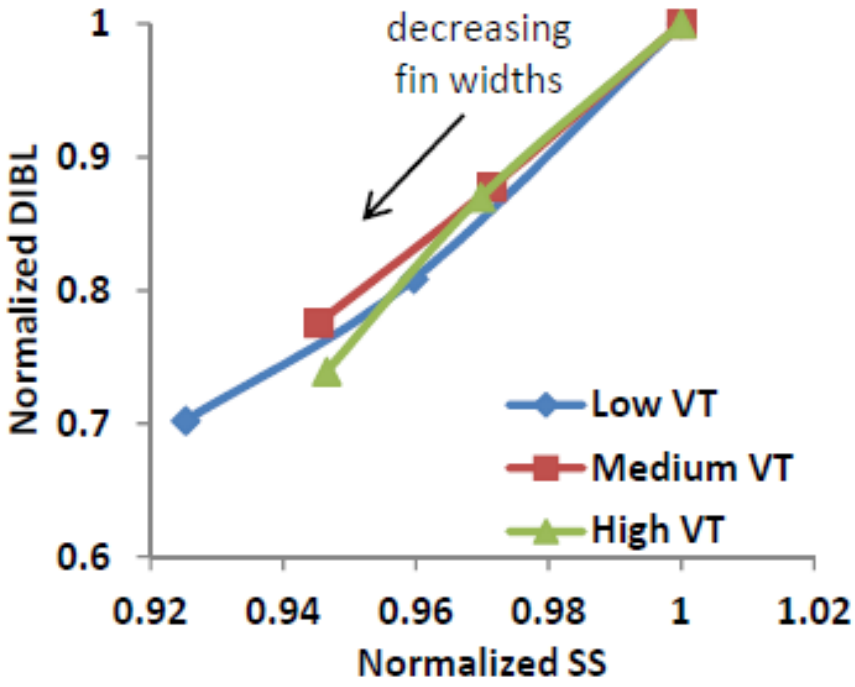
# Fin Height Scaling
## *Impact on SoC*




- Optimum Hfin exists for best SoC performance
  - Drive current vs. Total Capacitance trade-off

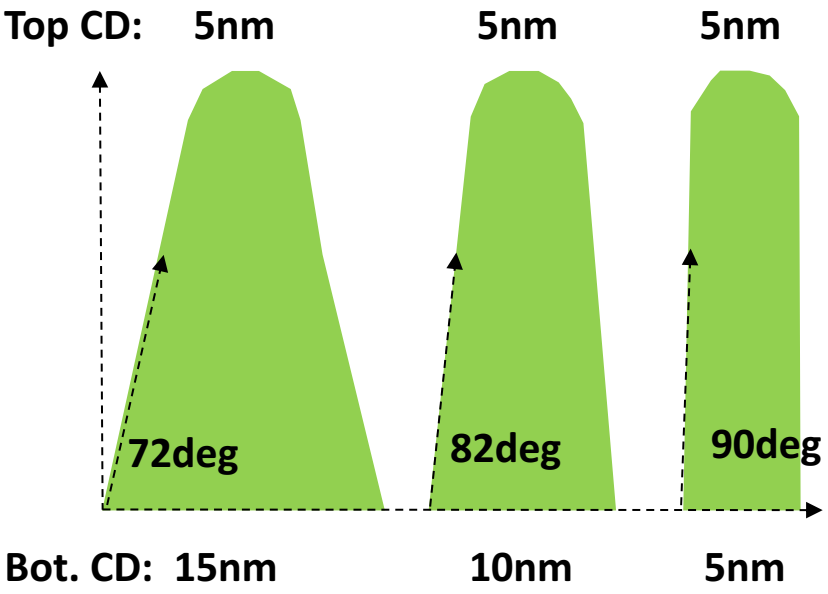
# Fin Width Scaling
## *Impact on SoC PPA*

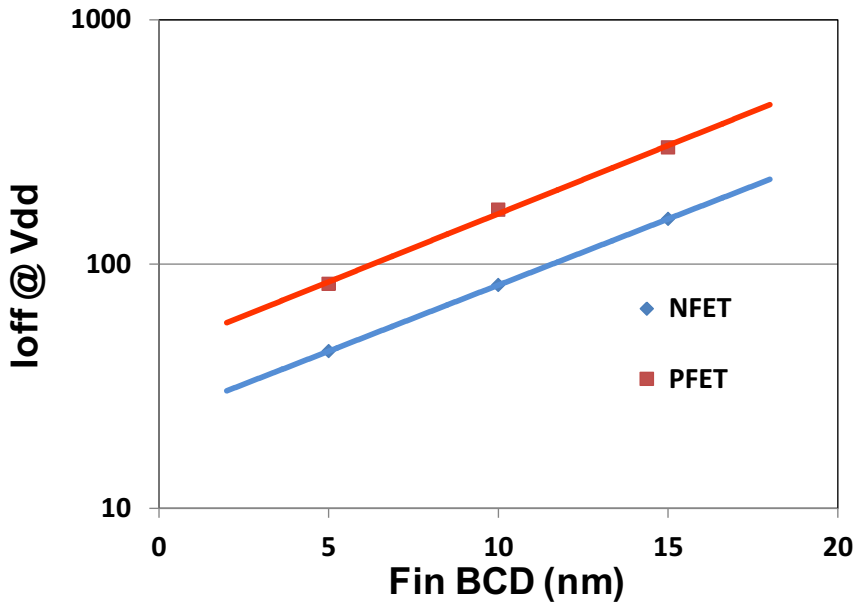



- Device electrostatics improve significantly with fin width scaling
- SoC stand-by leakage improves with Dfin scaling

# Fin Taper Scaling
## *Impact on SoC PPA*



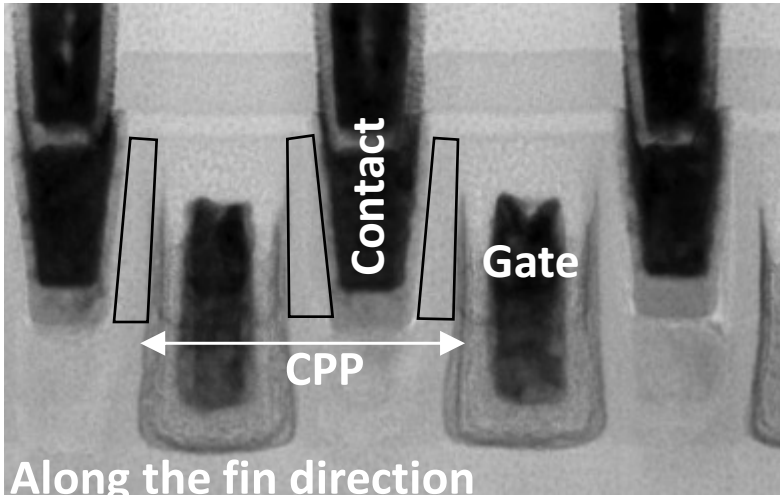




- Device electrostatics improve significantly with fin taper scaling
- SoC stand-by leakage improves with taper scaling

# Gate Pitch(CPP) Scaling
## *Goals*

CPP components:

- Gate Length
- Spacer thickness
- Contact CD

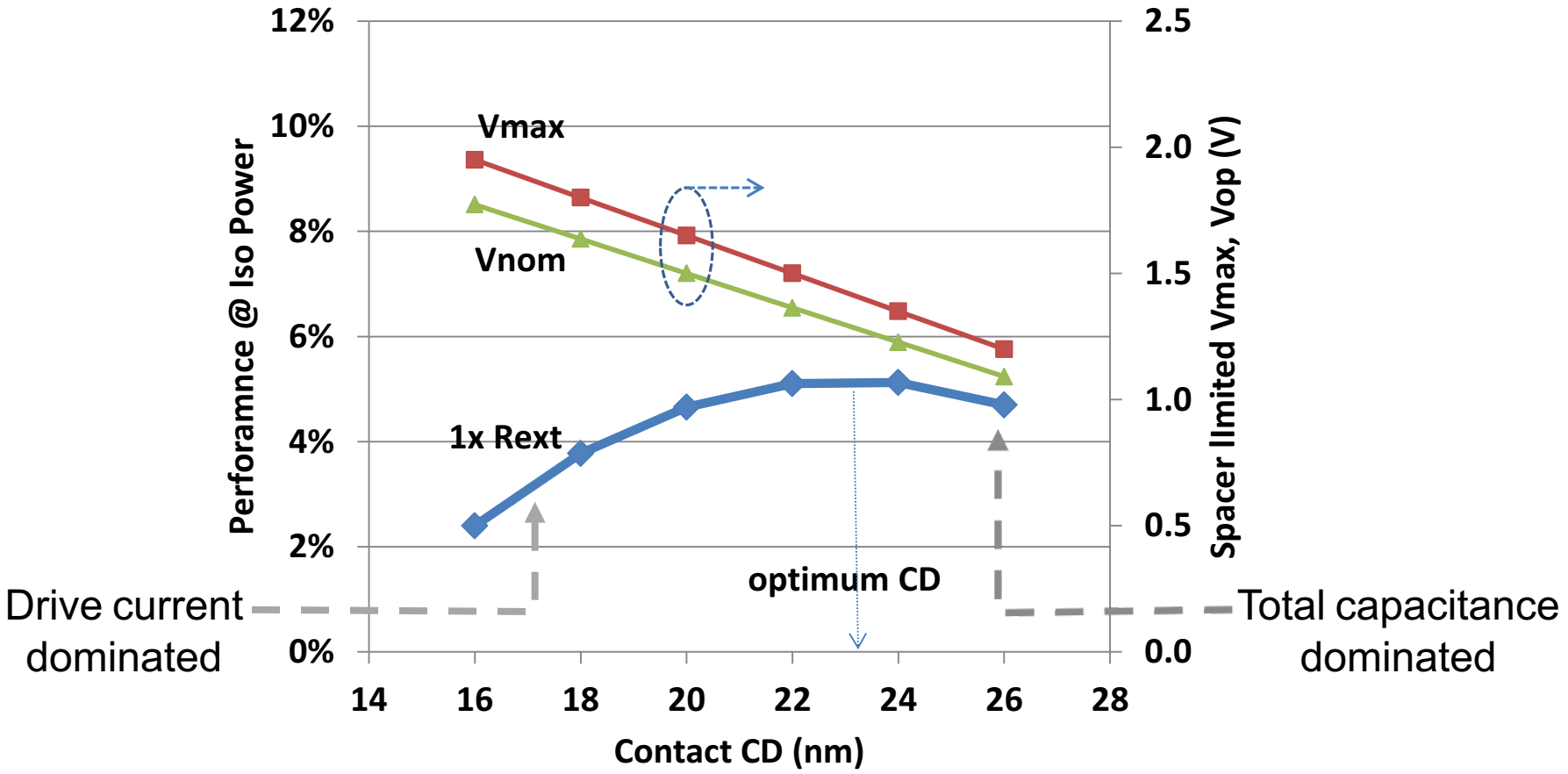



Goal of CPP Scaling

- Longer Lg → Best electrostatics, lower leakage
- Wider Contact CD → Best drive current
- Wider Spacer → Miller capacitance, Vmax and reliability

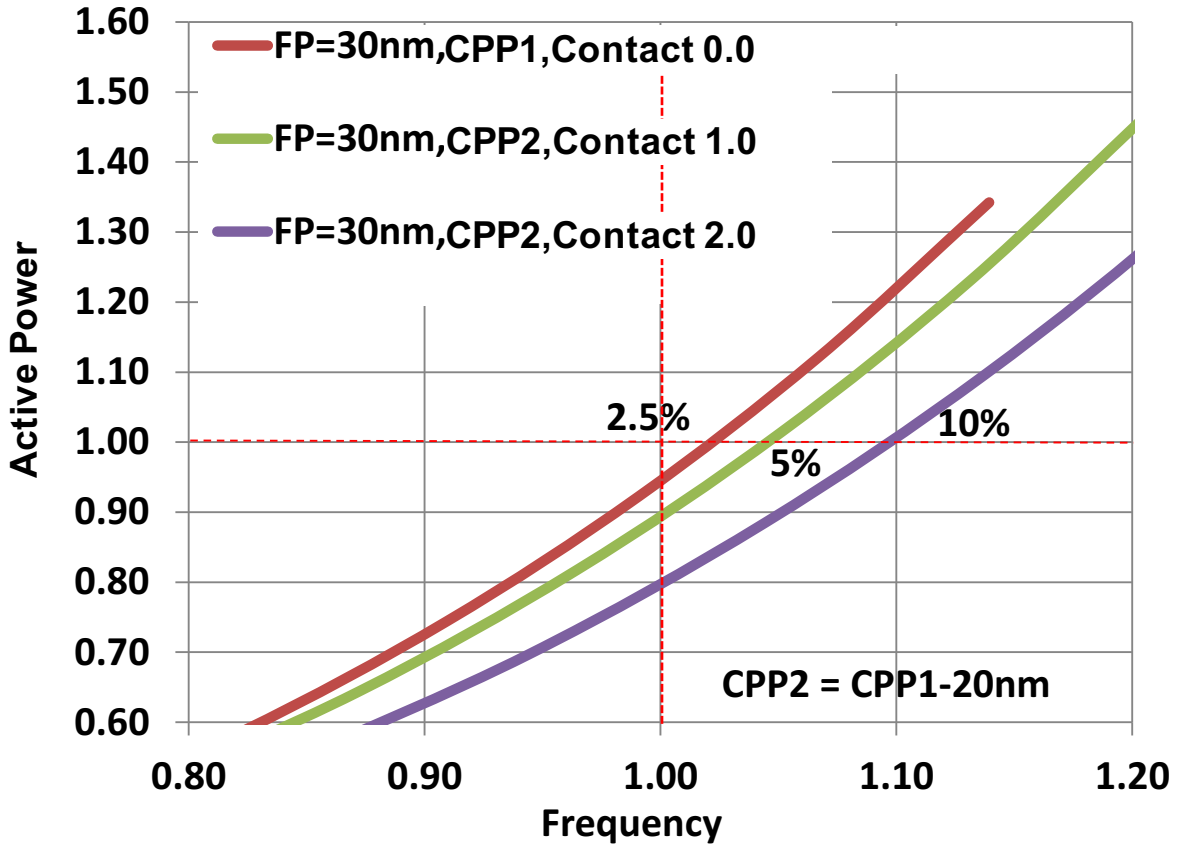
# Gate Pitch Scaling

## *Spacer vs. Contact CD*




- Optimize spacer & contact CD for best SoC performance

# Overall Scaling
## *Impact on SoC Performance*



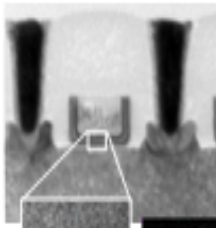

- Fin and CPP Scaling drives innovation in parasitics reduction (Rext, Ceff) to meet SoC PPA

# Future Directions

| | |
|---|---|
| 1 | Innovation in device parasitic R & C reduction |
| 2 | FinFETs on Drugs: High Mobility Ch. Materials |
| 3 | New Device Architectures (FDSOI, GAA, TFET) |

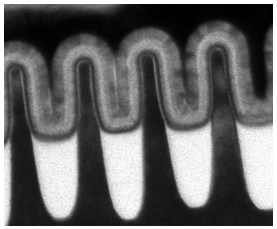
Challenges: Increasing Cost & Time to Market,

# Advanced Device Architectures

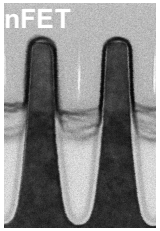


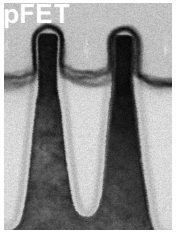
Planar

3D

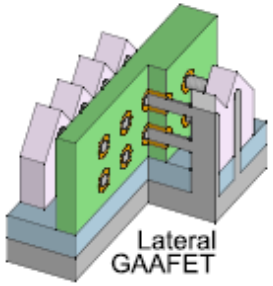


Si FinFET

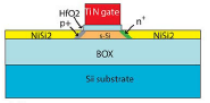


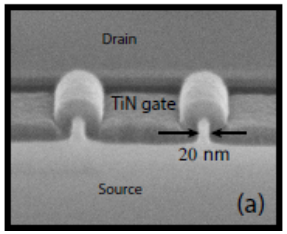




High Mobility Channel FinFET

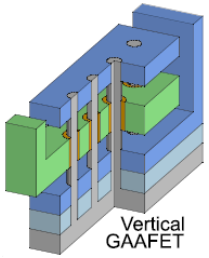



GAAFET

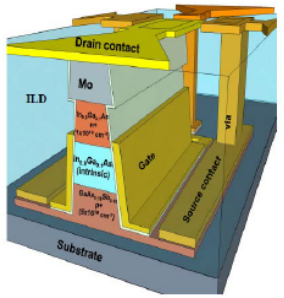





Lateral GAA TFET
Zhao, JEDS 2015

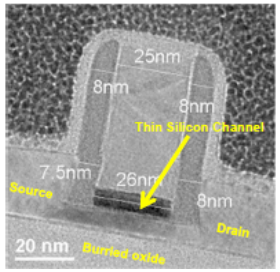



Yakimets
TED 2015

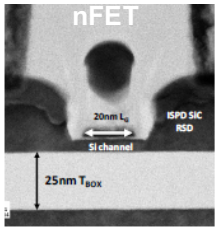


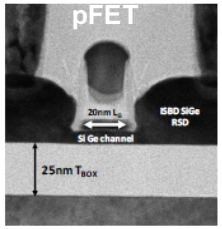

Vertical GAA TFET
Bijesh IEDM2013

2D

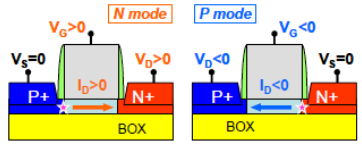



FDSOI




High Mobility Channel FDSOI
Qiu IEDM 2013




TFET
CEA-LETI VLSI 2012

# Summary

- Fin & Gate pitch scaling are increasing device parasitics (Rext, Rgate, Ceff) in scaled FinFETs
- Diminishing SoC PPA benefits on scaled FinFETs without optimizing device parasitics
- S/D design & Contact materials innovation on scaled FinFET are key to maximize SoC PPA benefits
- Novel materials & device architectures (GAA, TFET, FDSOI) are emerging to address scaling challenges

# Thank You

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